THE HONORABLE JAMES L. ROBART

UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF WASHINGTON
AT SEATTLE

SRC LABS, LLC & SAINT REGIS MOHAWK TRIBE, Plaintiffs, v. AMAZON WEB SERVICES, INC., AMAZON.COM, INC., & VADATA INC. Defendants.	Case No.: 2:18-cv-00317-JLR **JOINT CLAIM CHART AND PREHEARING STATEMENT** **JURY TRIAL DEMANDED**
SRC LABS, LLC & SAINT REGIS MOHAWK TRIBE, Plaintiffs, v. MICROSOFT CORPORATION, Defendant.	Case No.: 2:18-cv-00321-JLR **JURY TRIAL DEMANDED**

Plaintiffs SRC Labs, LLC & Saint Regis Mohawk Tribe (collectively, "SRC"), Defendants Amazon Web Services, Inc., Amazon.com, Inc., and VADATA Inc. (collectively "Amazon") and Defendant Microsoft Corp. ("Microsoft") submit this Joint Claim Chart and Prehearing Statement per Local Patent Rule 132, the Court's Standing Order for Patent Cases, the Court's May 23, 2018 Order consolidating *SRC Labs, LLC v. Amazon Web Servs. Inc.*, No. 2:18-cv-00317-JLR ("the

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Amazon case") and *SRC Labs, LLC v. Microsoft Corporation*, No.: 2:18-cv-00321-JLR ("the Microsoft case") for a *Markman* hearing and *Markman*-related pretrial matters (Dkt. 96[1]), and the Court's October 23, 2018 Order Modifying the Claim Construction Schedule (Dkt. 110).

SRC asserts four patents against Amazon and six patents against Microsoft. Two of the patents—U.S. Patent No. 7,225,324 (the "'324 patent") and U.S. Patent No. 7,620,800 (the "'800 patent")—are asserted against both Amazon and Microsoft. The remaining two patents that SRC asserts against Amazon are U.S. Patent No. 7,149,867 (the "'867 patent") and U.S. Patent No. 9,153,311 (the "'311 patent"). The remaining four patents that SRC asserts against Microsoft are U.S. Patent Nos. 6,434,687 (the "'687 patent"), 6,076,152 (the "'152 patent"), 6,247,110 (the "'110 patent"), and 7,421,524 (the "'524 patent").

I. SRC'S ALLEGATIONS OF INFRINGEMENT

A. Against Amazon

The table below identifies each claim of each patent-in-suit that SRC asserts in the Amazon case, and each apparatus, product, device, process, method, act, or other instrumentality that SRC accuses of infringing each asserted claim:

Patent Number	Asserted Claims	Applicable subsection of § 271	Accused Devices
7,149,867	1, 3, 4	§271(a)	EC2 F1 Instance
7,225,324	1, 17	§271(b)	Zebra and other similar applications designed to run on EC2 F1 Instance
7,620,800	1, 17	§271(b)	Zebra and other similar applications designed to run on EC2 F1 Instance
9,153,311	1, 3, 9, 10	§271(a)	EC2 F1 Instance

SRC believes each claim limitation is literally present in the accused devices. Amazon denies that it infringes any valid and enforceable claim directly or indirectly, literally or otherwise.

[1] Unless otherwise indicated, docket citations refer to the docket number in *SRC Labs, LLC v. Amazon Web Servs. Inc.*, No. 2:18-cv-00317-JLR.

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B. Against Microsoft

The table below identifies each claim of each patent in suit that Plaintiffs allege Microsoft is infringing, each accused apparatus, product, device, process, method, act, or other instrumentality accused of infringing each asserted claim, including for each claim the applicable statutory subsections of 35 U.S.C. § 271 asserted:

Patent Number	Asserted Claims	Applicable subsection of § 271	Accused Devices
6,076,152	1-7, 11, 12, 15, 21	§271(a)	Catapult v2 (Pikes Peak, Storey Peak), Catapult v3 (Dragontail Peak, Longs Peak, Nicholas Peak[2]), Catapult v4 (Storm Peak[3]).
6,247,110	1-7, 11, 12, 15, 21	§271(a)	Catapult v2 (Pikes Peak, Storey Peak), Catapult v3 (Dragontail Peak, Longs Peak, Nicholas Peak[4]), Catapult v4 (Storm Peak[5]).
6,434,687	1-5, 10-13, 18, 25	§271(a)	Bing (Ranking, Selection, DNN, CNN).
7,225,324	1, 8, 9, 17, 18, 21, 22, 23	§271(a)	Bing (Ranking, Selection, DNN, CNN), Brainwave, Azure Accelerated Networking, Compression (Xpress9 Level 6, Express8 Level 5), decompression, JPEG & video compression; LZ77 data compression, all applications running on the role or soft-shell portion of an FPGA in a Catapult Board.
7,421,524	1, 2, 13, 15	§271(a)	Catapult v2 (Pikes Peak, Storey Peak), Catapult v3 (Dragontail Peak, Longs Peak, Nicholas Peak), Catapult v4 (Storm Peak).
7,620,800	1, 8, 9, 17, 18, 21, 22, 23	§271(a)	Bing (Ranking, Selection, DNN, CNN), Brainwave, Azure Accelerated Networking, Compression (Xpress9 Level 6, Express8 Level 5), decompression, JPEG & video compression; LZ77 data compression, all applications running on the role or soft-shell portion of an FPGA in a Catapult Board.

Plaintiffs contend that each claim limitation is literally present in the Accused Devices. To the extent certain elements are not found to be literally present in the Accused Devices, and depending on the Court's construction, Plaintiffs contend the following elements may also be present

[2] Only accused to the extent it was deployed before December 17, 2017.
[3] Only accused to the extent it was deployed before December 17, 2017.
[4] Only accused to the extent it was deployed before December 17, 2017.
[5] Only accused to the extent it was deployed before December 17, 2017.

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under the doctrine of equivalents:

Patent Number	Claim	Term
6,076,152	1, 3, 11	Memory bank
6,247,110	1, 3, 11	Memory bank
6,076,152	1, 11	Memory addressable
6,247,110	1, 11	Memory addressable
7,421,524	1, 15	Memory module bus

Copies of the eight patents in suit are attached as Exhibits A-H and excerpts from the file histories are attached as Exhibits I-P, which are shown in the Table Below:

Exhibit A:	U.S. Patent No. 6,247,110
Exhibit B:	U.S. Patent No. 6,076,152
Exhibit C:	U.S. Patent No. 9,153,311
Exhibit D:	U.S. Patent No. 7,225,324
Exhibit E:	U.S. Patent No. 7,421,524
Exhibit F:	U.S. Patent No. 6,434,687
Exhibit G:	U.S. Patent No. 7,620,800
Exhibit H:	U.S. Patent No. 7,149,867
Exhibit I:	‘110 File History (excerpted pages)
Exhibit J:	‘152 File History (excerpted pages)
Exhibit K:	‘311 File History (excerpted pages)
Exhibit L:	‘324 File History (excerpted pages)
Exhibit M:	‘524 File History (excerpted pages)
Exhibit N:	‘687 File History (excerpted pages)
Exhibit O:	‘800 File History (excerpted pages)
Exhibit P:	‘867 File History (excerpted pages)

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II. AMAZON'S ALLEGATIONS OF INVALIDITY

Amazon contends that all asserted claims of each of the patents that SRC asserts against Amazon—the '324 patent, the '800 patent, the '867 patent, and the '311 patent—are invalid. The table below identifies the claims that Amazon alleges are invalid. Amazon served Invalidity Contentions served on July 9, 2018 and Amended Invalidity Contentions served on October 3, 2018. Included in the table below are the bases of the alleged invalidity and the relevant prior art as provided in those Contentions:

Patent	Claims	Bases of Invalidity	Relevant Prior Art Under §§ 102, 103
'324 patent	1, 17	The claims are invalid under 35 U.S.C. §§ 102, 103, 112 as anticipated, obvious, indefinite, and lacking written description and/or enablement.	• U.S. Patent No. 6,438,747 B1 ("Schreiber") • U.S. Patent No. 5,361,367 ("Fijany") • U.S. Patent No. 7,139,743 B2 ("Indeck") • U.S. Patent No. 6,675,187 B1 ("Greenberger") • "Building and Using a Highly Parallel Programmable Logic Array," Gokhale et al., January 1991 ("Splash") • An FPGA Implementation of Walsh-Hadamard Transforms for Signal Processing," A. Amira et al., 2001 ("Amira") • U.S. Patent No. 5,757,959 ("Lopresti") • U.S. Patent No. 4,698,751 ("Parvin") • "Artificial Neural Network Implementation on a single FPGA of a Pipelined On-Line Backpropagation," R. Gadea et al, Proceedings of International Symposium on Systems Synthesis, 2000 ("Gadea") • "Searching Genetic Databases on Splash 2," D. Hoang, 1993 ("Hoang") • "Mapping Nested Loops to Field Programmable Gate Array Based Systems," J. Spillane and J.S.N. Jean, NAECON 1995 ("Spillane") • "Splash 2: FPGAs in a Custom Computing Machine," D.A. Buell et al., 1996 ("Buell")

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Patent	Claims	Bases of Invalidity	Relevant Prior Art Under §§ 102, 103
			• "Evaluation of the Streams-C C-to-FPGA Compiler: An Applications Perspective," J. Frigo et al., February 11-13, 2001 ("Streams-C") • "PCI-based WILDFIRE Reconfigurable Computing Engines," by B. K. Fross et al., October 21, 1996 ("Fross")
'800 patent	1, 17	The claims are invalid under 35 U.S.C. §§ 102, 103, 112 as anticipated, obvious, indefinite, and lacking written description and/or enablement.	• U.S. Patent No. 5,361,367 ("Fijany") • U.S. Patent No. 7,139,743 B2 ("Indeck") • U.S. Patent No. 6,438,747 B1 ("Schreiber") • U.S. Patent No. 6,675,187 B1 ("Greenberger") • "Building and Using a Highly Parallel Programmable Logic Array," Gokhale et al., January 1991 ("Splash") • An FPGA Implementation of Walsh-Hadamard Transforms for Signal Processing," A. Amira et al., 2001 ("Amira") • U.S. Patent No. 5,757,959 ("Lopresti") • U.S. Patent No. 4,698,751 ("Parvin") • "Artificial Neural Network Implementation on a single FPGA of a Pipelined On-Line Backpropagation," R. Gadea et al, Proceedings of International Symposium on Systems Synthesis, 2000 ("Gadea") • "Searching Genetic Databases on Splash 2," D. Hoang, 1993 ("Hoang") • "Mapping Nested Loops to Field Programmable Gate Array Based Systems," J. Spillane and J.S.N. Jean, NAECON 1995 ("Spillane") • "Splash 2: FPGAs in a Custom Computing Machine," D.A. Buell et al., 1996 ("Buell") • "Evaluation of the Streams-C C-to-FPGA Compiler: An Applications Perspective," J. Frigo et al., February 11-13, 2001 ("Streams-C") • "PCI-based WILDFIRE Reconfigurable Computing Engines," by B. K. Fross et al., October 21, 1996 ("Fross")

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Patent	Claims	Bases of Invalidity	Relevant Prior Art Under §§ 102, 103
'311 patent	1, 3, 9, 10	The claims are invalid under 35 U.S.C. §§ 102, 103, 112 as anticipated, obvious, and indefinite.	• U.S. Patent Application Publication No. 2004/0034732 A1 ("Valin") • U.S. Patent Application Publication No. 2003/0200382 A1 ("Wells") • U.S. Patent No. 6,119,200 ("George") • U.S. Patent Application Publication No. 2014/0043918 A1 ("Ellis") • External Memory Interface Handbook Volume 3: Section III. DDR2 and DDR3 SDRAM Controller with UniPHY User • Guide, Altera, June 2011 ("UniPHY") • DDR2SOFT DDR2 Memory Controller VHDL Source Code Overview, ComBlock, September 22, 2010 ("ComBlock") • Atria DDR I/II DRAM Controller Core, Atria Logic Inc., 2009 ("Atria") • Xilinx MIG Spartan-6 MCB ("Spartan-6") • U.S. Patent No. 8,683,166 B1 ("Flateau") • ZedBoard System with Zync-7000 Processor ("ZedBoard + Zynq") • U.S. Patent Application Publication No. 2011/0264934 A1 ("Branover") • "System- and application-level support for runtime hardware reconfiguration on SoC platforms," Syrivelis et al., 2006 ("Syrivelis") • U.S. Patent No. 7,836,331 B1 ("Totolos") • "SUZAKU Hardware Manual," Atmark Techno, Inc., December 14, 2004 ("SUZAKU") • U.S. Patent No. 8,476,926 B2 ("Brunham") • "JEDEC Standard," JEDEC Solid State Technology Association, November 2008 ("JEDEC")
'867 patent	1, 3, 4	The claims are invalid under 35 U.S.C. §§ 102, 103, 112 as anticipated, obvious, and indefinite.	• U.S. Patent No. 6,822,959 B2 ("Galbi") • U.S. Patent No. 7,055,016 B2 ("Phelps") • "Memory Access Schemes for Configurable Processors," H. Lange and A. Koch, FPL 2000: Field-Programmable Logic and

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Patent	Claims	Bases of Invalidity	Relevant Prior Art Under §§ 102, 103
			Applications: The Roadmap to Reconfigurable Computing, 2000 ("Lange") • "Architectural Adaptation for Application-Specific Locality Optimizations," Xingbin Zhang et al., International Conference on Computer Design VLSI in Computers and Processors, 1997 ("Zhang") • U.S. Patent No. 6,662,285 B1 ("Douglass") • U.S. Patent No. 6,981,099 B2 ("Paulraj") • "An FPGA Implementation of Triangle Mesh Decompression," by Tulika Mitra ("Mitra") • U.S. Patent No. 6,182,206 B1 ("Baxter")

III. MICROSOFT'S ALLEGATIONS OF INVALIDITY

Microsoft contends that all asserted claims of each of the patents that SRC asserts against Microsoft—the '152 Patent, the '110 patent, the '324 patent, the '800 patent, the '687 patent, and the '524 patent—are invalid. The table below identifies the claims that Microsoft alleges are invalid, along with the bases of the alleged invalidity and the relevant prior art:

Patent	Claims	Bases of Invalidity	Relevant Prior Art Under §§ 102, 103
'152 patent	1-7, 11, 12, 15, 18, 21	The claims are invalid under 35 U.S.C. §§ 101, 102, 103, 112 as directed to an abstract idea, anticipated, obvious, indefinite, and lacking written description and/or enablement.	• US Patent No. 5,574,930 to Halverson et al. (issued November 12, 1996). • Halverson, Richard Peyton, Jr., Ph.D, The Functional Memory Approach to the Design of Custom Computing Machines, August 1994. • The pre-critical date or pre-invention date public use, public knowledge, offer for sale, sale or prior invention of any version of the machine described in the two references cited above. • U.S. Patent No. 5,678,021 by Pawate et al. (issued October 14, 1997). • U.S. Patent No. 6,185,704 by Pawate et al. (issued February 6, 2001, provisional filed

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Patent	Claims	Bases of Invalidity	Relevant Prior Art Under §§ 102, 103
			April 11, 1997). • "YARDS: FPGA/MPU Hybrid Architecture for Telecommunication Data Processing" Tsutsui et al. • The pre-critical date or pre-invention date public use, public knowledge, offer for sale, sale or prior invention of any version of the YARDS and/or ANT devices described in the reference cited above. • U.S. Patent No. 6,470,380 by Yoshizawa et al. (issued October 22, 2002, filed October 21, 1997). • "Splash 2: FPGAs in a custom Computing Machine," D.A. Buell, J. M. Arnold, and W. J. Kleinfelder, IEEE Computer Society, 1996. • The pre-critical date or pre-invention date, public knowledge, offer for sale, sale or prior invention of any version of the Splash 2 system described in the reference cited above. • Prism II: "PRISM-II Compiler and Architecture," M. Wazlowski et al., in Proceedings of the IEEE Workshop on FPGAs for Custom Computing Machines. 5-7 April, 1993. • The pre-critical date or pre-invention date pubic use, public knowledge, offer for sale, sale or prior invention of any version of the PRISM-II system described in the reference cited above. • U.S. Patent No. 5,671,355 to Collins (issued September 23, 1997). • The pre-critical date or pre-invention date public use, public knowledge, offer for sale, sale or prior invention of any version of the Collins system described in the reference cited above. • U.S. Patent No. 5,835,734 to Alkalaj (issued November 10, 1998). • The pre-critical date or pre-invention date public use, public knowledge, offer for sale, sale or prior invention of any version

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Patent	Claims	Bases of Invalidity	Relevant Prior Art Under §§ 102, 103
			of the Alkalaj system described in the reference cited above • "Programmable Active Memories: Reconfigurable Systems Come of Age" by Vuillemin et al. ("Vuillemin")
'110 patent	1-7, 11, 12, 15, 18, 21	The claims are invalid under 35 U.S.C. §§ 101, 102, 103, 112 as directed to an abstract idea, anticipated, obvious, indefinite, and lacking written description and/or enablement.	• US Patent No. 5,574,930 to Halverson et al. (issued November 12, 1996). • Halverson, Richard Peyton, Jr., Ph.D, The Functional Memory Approach to the Design of Custom Computing Machines, August 1994. • The pre-critical date or pre-invention date public use, public knowledge, offer for sale, sale or prior invention of any version of the machine described in the two references cited above. • U.S. Patent No. 5,678,021 by Pawate et al. (issued October 14, 1997). • U.S. Patent No. 6,185,704 by Pawate et al. (issued February 6, 2001, provisional filed April 11, 1997). • "YARDS: FPGA/MPU Hybrid Architecture for Telecommunication Data Processing" Tsutsui et al. • The pre-critical date or pre-invention date public use, public knowledge, offer for sale, sale or prior invention of any version of the YARDS and/or ANT devices described in the reference cited above. • U.S. Patent No. 6,470,380 by Yoshizawa et al. (issued October 22, 2002, filed October 21, 1997). • "Splash 2: FPGAs in a custom Computing Machine," D.A. Buell, J. M. Arnold, and W. J. Kleinfelder, IEEE Computer Society, 1996. • The pre-critical date or pre-invention date, public knowledge, offer for sale, sale or prior invention of any version of the Splash 2 system described in the reference cited above.

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Patent	Claims	Bases of Invalidity	Relevant Prior Art Under §§ 102, 103
			• Prism II: "PRISM-II Compiler and Architecture," M. Wazlowski et al., in Proceedings of the IEEE Workshop on FPGAs for Custom Computing Machines. 5-7 April, 1993. • The pre-critical date or pre-invention date pubic use, public knowledge, offer for sale, sale or prior invention of any version of the PRISM-II system described in the reference cited above. • U.S. Patent No. 5,671,355 to Collins (issued September 23, 1997). • The pre-critical date or pre-invention date public use, public knowledge, offer for sale, sale or prior invention of any version of the Collins system described in the reference cited above. • U.S. Patent No. 5,835,734 to Alkalaj (issued November 10, 1998). • The pre-critical date or pre-invention date public use, public knowledge, offer for sale, sale or prior invention of any version of the Alkalaj system described in the reference cited above • "Programmable Active Memories: Reconfigurable Systems Come of Age" by Vuillemin et al. ("Vuillemin")
'324 patent	1, 8, 9, 17, 18, 21, 22, 23	The claims are invalid under 35 U.S.C. §§ 101, 102, 103, 112 as directed to an abstract idea, anticipated, obvious, indefinite, and lacking written description and/or enablement.	• "Splash 2: FPGAs in a custom Computing Machine," D.A. Buell, J. M. Arnold, and W. J. Kleinfelder, IEEE Computer Society, 1996. • The pre-critical date or pre-invention date public use, public knowledge, offer for sale, sale or prior invention of any version of the Splash 2 system described in the reference cited above. • "Evaluation of the Streams-C C-to-FPGA Compiler: An Applications Perspective," J. Frigo et al., in Proceedings of the Association for Computing Machinery (ACM), February 11-13, 2001. • "PCI-based WILDFIRE Reconfigurable Computing Engines," B. K. Fross et al., in

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Patent	Claims	Bases of Invalidity	Relevant Prior Art Under §§ 102, 103
			Proceedings of the International Society for Optics and Photonics (SPIE) Vol. 2914, October 21, 1996. • The pre-critical date or pre-invention date public use, public knowledge, offer for sale, sale or prior invention of any version of the WILDFIRE system described in the reference cited above. • U.S. Patent No. 6,182,206,"Dynamically Reconfigurable Computing using a Processing Unit Having Changeable Internal Hardware Organization," filed February 26, 1998; priority date April 17, 1995. • "REMARC: Reconfigurable Multimedia Array Coprocessor," T. Miyamori and K. Olukotun, in IEICE Transactions on Information and Systems E82-D, Volume 82, pages 389-397, 1998. • The pre-critical date or pre-invention date public use, public knowledge, offer for sale, sale or prior invention of any version of the REMARC system described in the reference cited above. • "Computing Multidimensional DFTs Using Xilinx FPGAs," C. Dick, in Proceedings of the 8th International Conference on Signal Processing Applications and Technology, September 13-16, 1998 • "The Fast Fourier Transform on a Reconfigurable Processor," G. Donohoe, J. Purviance, and P. Yeh, in Proceedings of the NASA Earth Sciences Technology Conference, June 11-13, 2002. • U.S. Patent No. 6,883,084 (issued on April 19, 2005, provisional filed July 25, 2001). • Mapping Applications to the RaPiD Configurable Architecture to C. Ebeling et al. • Data-Driven Multicomputers to J. Gaudiot • Automated Target Recognition on Splash 2, Rencher, et al.

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Patent	Claims	Bases of Invalidity	Relevant Prior Art Under §§ 102, 103
			• Development of a parallel molecular dynamics code on SIMD Computers: Algorithm for use of pair list criterion to Roccatano, et al.
'800 patent	1, 8, 9, 17, 18, 21, 22, 23	The claims are invalid under 35 U.S.C. §§ 101, 102, 103, 112 as directed to an abstract idea, anticipated, obvious, indefinite, and lacking written description and/or enablement.	• "Splash 2: FPGAs in a custom Computing Machine," D.A. Buell, J. M. Arnold, and W. J. Kleinfelder, IEEE Computer Society, 1996. • The pre-critical date or pre-invention date public use, public knowledge, offer for sale, sale or prior invention of any version of the Splash 2 system described in the reference cited above. • "Evaluation of the Streams-C C-to-FPGA Compiler: An Applications Perspective," J. Frigo et al., in Proceedings of the Association for Computing Machinery (ACM), February 11-13, 2001. • "PCI-based WILDFIRE Reconfigurable Computing Engines," B. K. Fross et al., in Proceedings of the International Society for Optics and Photonics (SPIE) Vol. 2914, October 21, 1996. • The pre-critical date or pre-invention date public use, public knowledge, offer for sale, sale or prior invention of any version of the WILDFIRE system described in the reference cited above. • U.S. Patent No. 6,182,206,"Dynamically Reconfigurable Computing using a Processing Unit Having Changeable Internal Hardware Organization," filed February 26, 1998; priority date April 17, 1995. • "REMARC: Reconfigurable Multimedia Array Coprocessor," T. Miyamori and K. Olukotun, in IEICE Transactions on Information and Systems E82-D, Volume 82, pages 389-397, 1998. • The pre-critical date or pre-invention date public use, public knowledge, offer for sale, sale or prior invention of any version of the REMARC system described in the

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Patent	Claims	Bases of Invalidity	Relevant Prior Art Under §§ 102, 103
			reference cited above. • "Computing Multidimensional DFTs Using Xilinx FPGAs," C. Dick, in Proceedings of the 8th International Conference on Signal Processing Applications and Technology, September 13-16, 1998 • "The Fast Fourier Transform on a Reconfigurable Processor," G. Donohoe, J. Purviance, and P. Yeh, in Proceedings of the NASA Earth Sciences Technology Conference, June 11-13, 2002. • U.S. Patent No. 6,883,084 (issued on April 19, 2005, provisional filed July 25, 2001). • Mapping Applications to the RaPiD Configurable Architecture to C. Ebeling et al. • Data-Driven Multicomputers to J. Gaudiot • Automated Target Recognition on Splash 2, Rencher, et al. • Development of a parallel molecular dynamics code on SIMD Computers: Algorithm for use of pair list criterion to Roccatano, et al.
'687 patent	1-5, 10-13, 18, 25	The claims are invalid under 35 U.S.C. §§ 101, 102, 103, 112 as directed to an abstract idea, anticipated, obvious, indefinite, and lacking written description and/or enablement.	• "The Architecture of the Obelix - An Improved Internet Search Engine," P. Knezevic et al., Naval Postgraduate School, Proceedings of the 33rd Annual Hawaii International Conference on System Sciences (HICSS) Jan. 4-7, 2000, Maui, HI, USA, pp. 2145-2155 • The pre-critical date or pre-invention date public use, public knowledge, offer for sale, sale, or prior invention or, or derivation from, of any version of the Obelix system described in the three references cited above. • U.S. Patent No. 6,326,806 H. Fallside et al. (issued December 4, 2001, filed March 29, 2000). • The pre-critical date or pre-invention date public use, public knowledge, offer for sale, sale, or prior invention of any version

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Patent	Claims	Bases of Invalidity	Relevant Prior Art Under §§ 102, 103
			of the Fallside system described in the reference cited above. • "A Web Based Multiuser Operating System for Reconfigurable Computing," to O. Diessel et al. in Proceedings of the Association for Computing Machinery (ACM), published during a conference held on April 12-16, 1999 • The pre-critical date or pre-invention date public use, public knowledge, offer for sale, sale, or prior invention of any version of the Space 2 system described in the reference above. • "Networking Requirements and Solutions for a TV WWW Browser," to T. David et al., submitted to the Virginia Polytechnic Institute and State University on September 17, 1997 • U.S. Patent No. 6,370,527 to A. Singhal et al. (issued April 9, 2002, filed December 29, 1998) • U.S. Patent No. 6,795,448 to P. Lee et al. (issued September 21, 2004, filed March 2, 2000) • U.S. Patent No. 5,887,165 to S. Martel et al. (issued March 23, 1999) • U.S. Patent No. 6,101,180 to P. Donahue et al. (issued August 8, 2000) • U.S. Patent No. 5,870,769 to Y. Freund (issued February 9, 1999) • A press release entitled "Xilinx Unveils Internet Reconfigurable Logic," ("Xilinx Press Release"), published on November 10, 1998. • "An Open Platform for Development of Network Processing Modules in Reprogrammable Hardware," to J. Lockwood in IEC DesignCon 2001 ("FPX"), published during a conference held in January of 2001. • A dynamic reconfiguration run-time system to J. Burns et al. • U.S. Patent No. 7,072,888 to A. Perkins

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Patent	Claims	Bases of Invalidity	Relevant Prior Art Under §§ 102, 103
			(issued July 4, 2006, filed June 16, 1999). • U.S. Patent No. 6,230,307 to D. Davis et al. (issued May 8, 2001). • U.S. Patent No. 6,098,065 to R. Skillen et al. (issued August 1, 2000).
'524 patent	1, 2, 13, 14, 15	The claims are invalid under 35 U.S.C. §§ 101, 102, 103, 112 as directed to an abstract idea, anticipated, obvious, indefinite, and lacking written description and/or enablement.	• "YARDS: FPGA/MPU Hybrid Architecture for Telecommunication Data Processing" Akihiro Tsutsui and Toshiaki Miyazaki, FPGA '97 ("Tsutsui"), presented and published at the 1997 ACM Fifth International Symposium on Field-Programmable Gate Arrays in California on February 9-11, 1997. • The pre-critical date or pre-invention date public use, public knowledge, offer for sale, sale or prior invention of any version of the YARDS and/or ANT devices described in the reference cited above. • "Pilchard—A Reconfigurable Computing Platform With Memory Slot Interface," P. H. W. Leong, M. P. Leong, O. Y. H. Cheung, et al.,, in Proceedings of the 9th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM '01), pp. 170–179, Rohnert Park, California, USA, April 29, 2001-May 2, 2001. • The pre-critical date or pre-invention date public use, public knowledge, offer for sale, sale or prior invention of any version of the Pilchard system described in the reference cited above. • U.S. Patent No. 5,671,355 to Collins (issued September 23, 1997). • The pre-critical date or pre-invention date public use, public knowledge, offer for sale, sale or prior invention of any version of the Collins system described in the reference cited above. • U.S. Patent No. 5,835,734 to Alkalaj et al. (issued on November 10, 1998, filed on September 23, 1997)

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Patent	Claims	Bases of Invalidity	Relevant Prior Art Under §§ 102, 103
			• Special purpose FPGA for High-Speed Digital Telecommunication Systems to Tsutsui, et al. • Reconfigurable Real-Time Signal Transport System using Custom FPGAs to Hyashi et al. • U.S. Patent No. 5,857,109 to Taylor • Microcomputer Interfacing to Harold Stone

IV. AGREED CONSTRUCTIONS

SRC and Amazon have agreed to the constructions of the following claim terms:

Claim Terms	Agreed Constructions
"A method for data processing in a reconfigurable computing system, the reconfigurable computing system comprising at least one reconfigurable processor, the reconfigurable processor comprising a plurality of functional units, said method comprising" – '324 patent, claim 1	The preamble is limiting.
"A method for data processing in a reconfigurable computing system, the reconfigurable computing system comprising at least one reconfigurable processor, the reconfigurable processor comprising a plurality of functional units, said method comprising" –'800 patent, claim 1	The preamble is limiting.
"a data driven calculation" –'800 Patent, claim 1	Computation triggered by the availability of input data
"reconfigurable logic device" – '311 patent, claims 1, 3, 9, 10	FPGA, hybrid devices, such as a reconfigurable logic device with partial reconfiguration capabilities or an application specific integrated circuit (ASIC) device with reprogrammable regions contained within the chip

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"A reconfigurable processor that instantiates an algorithm as hardware comprising" – '867 patent, claim 1	The preamble is limiting.

SRC and Microsoft have agreed to the constructions of the following claim terms:

Claim Terms	Agreed Constructions
Preamble of Claim 1 - `324 Patent and `800 Patent	The preamble is a claim limitation.
"Addressable" - `152 Patent: 1 & `110 Patent: 1	Accessible using normal memory access protocols
"Addressed" - `152 Patent: 1 & `110 Patent: 1	Accessed using normal memory access protocols
"Address" - `152 Patent: 1 & `110 Patent: 1	To access using normal memory access protocols
"a single system image of an operating system." - `687 Patent: 10, 11	an operating system that hides the heterogeneous and distributed nature of the available resources and presents them to the user and applications as a single unified computing resource
"Plurality" - `152 Patent: 1-7, 11, 12, 15, 18 and 21 & `110 Patent: 1-7, 11, 12, 15, 18 and 21	More than one
"instantiating" - `687 Patent: 1, 11	configuring

V. DISPUTED CLAIM TERMS

C. Patents Common to the Amazon Case and the Microsoft Case

With respect to the commonly asserted '324 and '800 patents, the parties in both cases dispute the claim constructions for the following three terms:

1. **"systolic" and "systolically"** – '324 patent: claim 1
2. **"pass computed data seamlessly"** – '324/'800 patents: claim 1

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3. **"instantiating," "instantiated," and "instantiation"** – '324 patent: claim 1

D. Patents Asserted Against Amazon Only

With respect to the two patents asserted against Amazon only (the '311 patent and the '867 patent), SRC and Amazon dispute the claim constructions for the following four terms:

1. **"a data maintenance block"** – '311 patent: claim 1
2. **"a data prefect unit"** – '867 patent: claims 1, 3, 4
3. **"a data prefetch unit coupled to the memory, wherein the data prefetch unit retrieves only computational data required by the algorithm from a second memory of second characteristic memory bandwidth and/or memory utilization and places the retrieved computational data in the first memory"** – '867 patent: claim 1
4. **"at least the first memory and data prefetch unit are configured to conform to needs of the algorithm"** – '867 patent: claims 1, 3, 4

E. Patents Asserted Against Microsoft Only

With respect to the four patents asserted against Microsoft only (the '687 patent, the '152 patent, the'110 patent, and the '524 patent), SRC and Microsoft dispute the claim constructions for the following ten terms:

1. **A data driven calculation** – '800 patent: claim 1
2. **Memory bank** – '152/'110 patents claims: 1, 3, 11, 20
3. **Memory algorithm processor/reconfigurable memory algorithm processor** – '152/'110 patents claims: 1, 3, 11
4. **Means connecting** … - '152/'110 patents: claim 1
5. **Means coupling** … - '152/'110 patents: claim 11
6. **Memory module bus** – '524 patent: claim 1
7. **Providing said altered data directly from said memory module bus to an external device coupled thereto** – '524 patent claim 1
8. **The order of the steps recited in claim 1** – '687 patent

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9. **At an internet site** – ’687 patent: claim 1, 18

10. **Demographic data** – ’687 patent: claim 5, 12, 13

Attached as Exhibit R is the Joint Claim Chart of SRC and Amazon and attached as Exhibit Q is the Joint Claim Chart of SRC and Microsoft. Each chart contains the corresponding parties’ proposed constructions for each disputed claim term, phrase, or clause, together with an identification of intrinsic and extrinsic evidence on which each party intends to rely to support or oppose the proposed constructions.

VI. THE TEN MOST IMPORTANT DISPUTED CLAIM TERMS

SRC and Amazon dispute the claim constructions of seven terms only.

SRC and Microsoft dispute the claim constructions of thirteen terms, three of which are common to Amazon. A list of the ten most important disputed claim terms is below:

1. **Means connecting** … - ’152/’110 patents: claim 1
2. **Means coupling** … - ’152/’110 patents: claim 11
3. **“instantiating,” “instantiated,” and “instantiation”** – ’324/’800 patents: claim 1
4. **“Providing said altered data directly from said memory module bus to an external device coupled thereto** – ’524 patent claim 1
5. **The order of the steps recited in claim 1** – ’687 patent
6. **At an internet site** – ’687 patent: claim 1, 18
7. **Memory algorithm processor/reconfigurable memory algorithm processor** – ’152/’110 patents claims: 1, 3, 11
8. “**memory bank”** – ’152/’110 patents claims 1, 3, 11, 20
9. **“systolic” and “systolically”** – ’324 patent: claim 1
10. **“memory module bus** – ’524 patent claim 1

VII. THE CLAIM CONSTRUCTION HEARING

Anticipated Length: Pursuant to this Court’s Minute Order (Dkt. 96), the parties antici-

pate that the Claim Construction hearing will take place over two days, with three portions addressing the following patents: (1) the commonly-asserted patents (the '324 patent and the '800 patent); (2) the patents asserted only in the Amazon case (the '311 patent and the '867 patent); and (3) the patents asserted only in the Microsoft case (the '687 patent, the '152 patent, the '110 patent, and the '524 patent).

The parties anticipate that portion (1) of the Claim Construction Hearing will last approximately 2 hours, to be evenly allocated among the parties. Counsel for each party (SRC, Amazon, Microsoft) intends to present argument for each disputed term from the commonly-asserted patents.

SRC and Amazon anticipate that portion (2) of the Claim Construction Hearing will last approximately 2 hours, to be evenly allocated among the parties.

SRC and Microsoft believe that portion (3) of the Claim Construction Hearing will last approximately 5 hours, to be evenly allocated among the parties.

Proposed Order of Presentation: The parties propose that the hearing proceed on a term-by-term basis, according to the order in the list of disputed terms provided above, and for each term, SRC presents first followed by Amazon and/or Microsoft.

Live Testimony: The parties agree that live testimony at the Claim Construction Hearing is not necessary.

Technical Tutorials: The parties believe a technical tutorial on the subject matter of the patents would be helpful for the Court. SRC would like to present its technical tutorial through the live presentation of one of the inventors. Amazon may present its technical tutorial through the live presentation of its technical expert, Dr. Brad Hutchings. Microsoft believes that a technical tutorial can be provided by counsel the first day of the Markman hearing, but to the extent the Court would hear a presentation from SRC's inventor, Microsoft may present its technical tutorial through a live presentation by its technical expert, Dr. Henry Houh. The parties agree that any tutorial is not evidence for claim construction.

SRC and Amazon agree that the tutorial should take place before the Claim Construction

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Hearing, but they have no preference as to whether it is scheduled for December 20, 2018 (the first day of the Claim Construction Hearing) or at another day prior to that. SRC and Amazon agree that 45 minutes is sufficient for each party to present its tutorial in its case. Microsoft prefers that the technical tutorial take place on December 20, 2018, but otherwise agrees that believes that 45 minutes is sufficient for each party to present its tutorial in its case

Prehearing Conference: SRC believes that a pre-hearing conference is necessary to address issues the parties anticipate may arise during or after claim construction briefing.

Amazon and Microsoft do not anticipate any issues to arise during or after claim construction briefing that may require a pre-hearing conference, but do not oppose SRC's request. Should the Court be so inclined, any issues can also be addressed (along with the tutorial) on December 20, 2018 before the Claim Construction Hearing commences on that day.

Independent Expert: The parties do not think the appointment of an independent expert is necessary.

Dated: November 1, 2018

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CERTIFICATE OF SERVICE

I hereby certify that on this 1st day of November 2018, I electronically filed the foregoing with the Clerk of the Court using the CM/ECF system, which will send notification of such filing to all counsel of record.

Dated: November 1, 2018 *s/ Karin B. Swope*

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